	Document ID	Issue Date	Pages	Title	Current OR
1	US 20060280272 A1	20061214	56	Data-level clock recovery	375/355
2	US 20060233291 A1	20061019	59	Partial response receiver with clock data recovery	375/355
3	US 20060222137 A1	20061005	8	STORAGE EFFICIENT SLIDING WINDOW SUM	375/371
4	US 20060222136 A1	20061005	10	Methods and apparatus for bit synchronizing data transferred across a multi-pin asynchronous serial interface	375/371
5	US 20060222135 A1	20061005	8	Methods and apparatus for digital linearization of an analog phase interpolator	375/371
6	US 20060188050 A1	20060824	19	System and method for adaptively deskewing parallel data signals relative to a clock	375/371
7	US 20060088137 A1	20060427	10	Multi-frequency clock stretching systems	375/371
8	US 20060002500 A1	20060105	18	Method and apparatus for recovering a clock signal	375/371
9	US 20060002499 A1	20060105	8	DRIFT COMPENSATION SYSTEM AND METHOD IN A CLOCK DEVICE OF AN ELECTRONIC CIRCUIT	375/371
10	US 20050286670 A1	20051229	8	Method of measuring jitter frequency response	375/371
11	US 20050271179 A1	20051208	22	Multi-strobe generation apparatus, test apparatus and adjustment method	375/371
12	US 20050243960 A1	20051103	10	Method of phase shifting bits in a digital signal pattern	375/371
13	US 20050058234 A1	20050317	55	Data-level clock recovery	375/371

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2	Garlepp; Bruno W. et al.
3	Wang; Cindy Chun et al.
4	Rahman; Mahibur et al.
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14	US 20050018798 A1	20050127	74	Voice and data exchange over a packet based network with timing recovery	375/355
15	US 20040252802 A1	20041216	32	Data transmission device and input/output interface circuit	375/371
16	US 20040240598 A1	20041202	16	Method and system for pattern-independent phase adjustment in a clock and data recovery (CDR) circuit	375/371
17	US 20040218705 A1	20041104	12	Phase rotator, phase rotation method and clock and data recovery receiver incorporating said phase rotator	375/355
18	US 20040202269 A1	20041014	18	Reception data synchronizing apparatus and method, and recording medium with recorded reception data synchronizing program	375/368
19	US 20040196937 A1	20041007	12	Apparatus and method for clock adjustment in receiver of communication system	375/355
20	US 20040125902 A1	20040701	20	Phase shifter, phase shifting method and skew compensation system for high-speed parallel signaling	375/371
21	US 20040125901 A1	20040701	56	Phase error correction circuit and receiver incorporating the same	375/368
22	US 20040101073 A1	20040527	27	Method and apparatus for estimating response characteristic, and receiving method and receiver utilizing the same	375/343
23	US 20040028164 A1	20040212	21	System and method for data transition control in a multirate communication system	375/371
24	US 20030185326 A1	20031002	25	Frequency drift and phase error compensation in a VOFDM receiver	375/371
25	US 20030161429 A1	20030828	8	Device and method for comma detection and word alignment in serial transmission	375/371
26	US 20030152181 A1	20030814	26	Delay locked loop synthesizer with multiple outputs and digital modulation	375/371

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15	Yamaguchi, Hisakatsu
16	Yin, Guangming
17	Cranford, Hayden Clavie JR. et al.
18	Shimawaki, Kazuhiro
19	Wang, Wen-Chi et al.
20	Nishimura, Shinji et al.
21	Nakahara, Hideki et al.
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27	US 20030058967 A1	20030327	32	Phase detectors in carrier recovery for offset QAM and VSB	375/327
28	US 20030058952 A1	20030327	24	Single-carrier to multi-carrier wireless architecture	375/260
29	US 20030058951 A1	20030327	26	Efficient pilot tracking method for OFDM receivers	375/260
30	US 20030002608 A1	20030102	12	Apparatus and method for communication link receiver having adaptive clock phase shifting	375/371
31	US 20020141522 A1	20021003	27	Method and apparatus for processing digitally sampled signals at a resolution finer than that of a sampling clock	375/355
32	US 20020009170 A1	20020124	21	Phase rotator and data recovery receiver incorporating said phase rotator	375/371
33	US 20010055331 A1	20011227	80	Multi-pair gigabit ethernet transceiver	375/216
34	US 20010046266 A1	20011129	149	Apparatus and method for scdma digital data transmission using orthogonal codes and head end modem with no tracking loops	375/259
35	US 20010038674 A1	20011108	110	MEANS AND METHOD FOR A SYNCHRONOUS NETWORK COMMUNICATIONS SYSTEM	375/355
36	US 7149269 B2	20061212	14	Receiver for clock and data recovery and method for calibrating sampling phases in a receiver for clock and data recovery	375/373
37	US 7123677 B2	20061017	8	Variable sampling data output circuit	375/371
38	US 7123660 B2	20061017	29	Method and system for deskewing parallel bus channels to increase data transfer rates	375/257
39	US 7116744 B2	20061003	51	Clock recovery circuit and receiver circuit for improving the error rate of signal reproduction	375/371
40	US 7116742 B2	20061003	27	Timing recovery system for a multi-pair gigabit transceiver	375/355

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28	Webster, Mark A. et al.
29	Thomson, John et al.
30	Glenn, Robert C. et al.
31	Colborne, Steven Francis et al.
32	Schmatz, Martin
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36	Cranford, Jr.; Hayden C. et al.
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41	US 7106820 B2	20060912	14	System and method for establishing word synchronization	375/365
42	US 7099424 B1	20060829	21	Clock data recovery with selectable phase control	375/370
43	US 7092474 B2	20060815	27	Linear phase detector for high-speed clock and data recovery	375/375
44	US 7092472 B2	20060815	53	Data-level clock recovery	375/371
45	US 7092468 B2	20060815	25	Timing recovery system for a multi-pair gigabit transceiver	375/355
46	US 7092466 B2	20060815	22	System and method for recovering and deserializing a high data rate bit stream	375/355
47	US 7079614 B2	20060718	9	Method of generating a measure of a mistiming and apparatus therefor	375/354
48	US 7065052 B1	20060620	14	Cell stream replicating device	370/252
49	US 7058152 B2	20060606	13	Method and apparatus for timing recovery in ADSL transceivers under a TCM-ISDN crosstalk environment	375/371
50	US 7054358 B2	20060530	57	Measuring apparatus and measuring method	375/226
51	US 7050522 B2	20060523	20	Phase rotator and data recovery receiver incorporating said phase rotator	375/371
52	US 7035325 B2	20060425	10	Jitter measurement using mixed down topology	375/226
53	US 7031420 B1	20060418	22	System and method for adaptively deskewing parallel data signals relative to a clock	375/371
54	US 7016344 B1	20060321	14	Time slot interchanging of time slots from multiple SONET signals without first passing the signals through pointer processors to synchronize them to a common clock	370/359
55	US 7010074 B2	20060307	51	Oversampling clock recovery having a high follow-up character using a few clock signals	375/371
56	US 6973149 B2	20051206	5	Arrangement for capturing data	375/364
57	US 6968026 B1	20051122	10	Method and apparatus for output data synchronization with system clock in DDR	375/371

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43	Cao; Jun
44	Stojanovic; Vladimir M.
45	Agazzi; Oscar E.
46	Hwang; Sakyun et al.
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58	US 6968024 B1	20051122	16	Apparatus and method for operating a master-slave system with a clock signal and a separate phase signal	375/354
59	US 6968021 B1	20051122	22	Synchronization method and apparatus for modems based on jointly iterative turbo demodulation and decoding	375/340
60	US 6941484 B2	20050906	14	Synthesis of a synchronization clock	713/500
61	US 6870410 B1	20050322	37	All digital power supply system and method that provides a substantially constant supply voltage over changes in PVT without a band gap reference voltage	327/149
62	US 6862296 B1	20050301	9	Receive deserializer circuit for framing parallel data	370/503
63	US 6853696 B1	20050208	26	Method and apparatus for clock recovery and data qualification	375/375
64	US 6853695 B1	20050208	10	System and method for deriving symbol timing	375/371
65	US 6850580 B1	20050201	20	Bit synchronizing circuit	375/355
66	US 6804257 B1	20041012	12	System and method for framing and protecting variable-lenght packet streams	370/471
67	US 6795515 B1	20040921	16	Method and apparatus for locating sampling points in a synchronous data stream	375/355
68	US 6775342 B1	20040810	53	Digital phase shifter	375/371
69	US 6771725 B2	20040803	75	Multi-pair gigabit ethernet transceiver	375/355
70	US 6768734 B2	20040727	10	Device and method for equalizing data delays	370/366
71	US 6765975 B2	20040720	7	Method and apparatus for a tracking data receiver compensating for deterministic jitter	375/371
72	US 6760389 B1	20040706	16	Data recovery for non-uniformly spaced edges	375/326
73	US 6744285 B2	20040601	10	Method and apparatus for synchronously transferring data across multiple clock domains	326/96
74	US 6741615 B1	20040525	37	Methods and apparatuses for synchronizing data conversion of sonet framed data	370/514

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59	White; Steven L. et al.
60	To; Hing Y. et al.
61	Doyle; James Thomas et al.
62	Desai; Chintan
63	Moser; James et al.
64	Betts; William Lewis et al.
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66	Benayoun; Alain et al.
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71	Dunning; David S. et al.
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75	US 6732205 B2	20040504	29	Serial/parallel conversion circuit, data transfer control device, and electronic equipment	710/71
76	US 6724849 B1	20040420	14	Method and apparatus for timing recovery in ADSL transceivers under a TCM-ISDN crosstalk environment	375/371
77	US 6711220 B1	20040323	15	Bit position synchronizer	375/354
78	US 6701140 B1	20040302	19	Digital receive phase lock loop with cumulative phase error correction and dynamically programmable correction rate	455/260
79	US 6690757 B1	20040210	16	High-speed interconnection adapter having automated lane de-skew	375/371
80	US 6683921 B1	20040127	47	Received-signal absolute phasing apparatus of receiver	375/331
81	US 6678342 B1	20040113	30	Absolute-phasing synchronization capturing circuit	375/362
82	US 6674794 B1	20040106	8	System and method for sampling phase adjustment by an analog modem	375/222
83	US 6643336 B1	20031104	16	DC offset and bit timing system and method for use with a wireless transceiver	375/343
84	US 6636573 B2	20031021	38	Precision timing generator system and method	375/355
85	US 6614864 B1	20030902	29	Apparatus for and method of adaptive synchronization in a spread spectrum communications receiver	375/371
86	US 6584163 B1	20030624	20	Shared data and clock recovery for packetized data	375/360
87	US 6560276 B1	20030506	36	Synchronization techniques using an interpolation filter	375/222
88	US 6522706 B1	20030218	8	Delay spread estimation for multipath fading channels	375/343
89	US 6522696 B1	20030218	16	Adaptive frequency correction in a wireless communications system, such as for GSM and IS54	375/262
90	US 6466589 B1	20021015	21	Apparatus for verifying data integrity and synchronizing ATM cell data format for processing	370/518
91	US 6463109 B1	20021008	32	Multiple channel adaptive data recovery system	375/355

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76	Long; Guozhu et al.
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79	Bunton; William P. et al.
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83	Hsieh; Hsiang-Tsuen et al.
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92	US 6459746 B2	20021001	76	Multi-pair gigabit ethernet transceiver	375/371
93	US 6430242 B1	20020806	22	Initialization system for recovering bits and group of bits from a communications channel	375/371
94	US 6430235 B1	20020806	17	Non-data-aided feedforward timing synchronization method	375/326
95	US 6393083 B1	20020521	14	Apparatus and method for hardware implementation of a digital phase shifter	375/371
96	US 6366604 B1	20020402	10	Compensation for phase errors caused by clock jitter in a CDMA communication system	375/146
97	US 6363129 B1	20020326	27	Timing recovery system for a multi-pair gigabit transceiver	375/355
98	US 6347128 B1	20020212	16	Self-aligned clock recovery circuit with proportional phase detector	375/376
99	US 6307905 B1	20011023	25	Switching noise reduction in a multi-clock domain transceiver	375/371
100	US 6307869 B1	20011023	12	System and method for phase recovery in a synchronous communication system	370/516
101	US 6304623 B1	20011016	39	Precision timing generator system and method	375/355
102	US 6288656 B1	20010911	14	Receive deserializer for regenerating parallel data serially transmitted over multiple channels	341/100
103	US 6275554 B1	20010814	9	Digital symbol timing recovery network	375/371
104	US 6246281 B1	20010612	9	Absolute phasing circuit	329/304
105	US 6236696 B1	20010522	34	Digital PLL circuit	375/376
106	US 6192093 B1	20010220	10	Enhanced CIMT coding system and method with automatic word alignment for simplex operation	375/371
107	US 6178213 B1	20010123	16	Adaptive data recovery system and methods	375/355
108	US 6178208 B1	20010123	6	System for recovery of digital data from amplitude and phase modulated line signals using delay lines	375/322
109	US 6163276 A	20001219	32	System for remote data collection	340/870.4

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96	Mohindra; Rishi
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110	US 6154497 A	20001128	10	Method and system for analog to digital conversion	375/247
111	US 6148046 A	20001114	24	Blind automatic gain control system for receivers and modems	375/345
112	US 6115433 A	20000905	54	Adaptively-equalized digital receiver with carrier tracking	375/326
113	US 6115075 A	20000905	67	Method and apparatus for adjusting dot clock signal	348/537
114	US 6111919 A	20000829	24	Synchronization of OFDM signals	375/260
115	US 6088410 A	20000711	11	False-synchronization detection device for bit-synchronous circuit of . .pi/4-shift DQPSK demodulator	375/354
116	US 6084931 A	20000704	22	Symbol synchronizer based on eye pattern characteristics having variable adaptation rate and adjustable jitter control, and method therefor	375/355
117	US 6081538 A	20000627	9	Resynchronization of data	370/503
118	US 6075832 A	20000613	17	Method and apparatus for deskewing clock signals	375/375
119	US 6058150 A	20000502	9	Method and apparatus for combined timing recovery, frame synchronization and frequency offset correction in a receiver	375/365
120	US 6038267 A	20000314	39	Digital demodulator, maximum-value selector, and diversity receiver	375/329
121	US 6038266 A	20000314	10	Mixed mode adaptive analog receive architecture for data communications	375/317
122	US 6031847 A	20000229	27	Method and system for deskewing parallel bus channels	370/508
123	US 6014417 A	20000111	12	On-chip phase step generator for a digital phase locked loop	375/374
124	US 6009132 A	19991228	34	System and method for obtaining clock recovery from a received data signal	375/355
125	US 6002731 A	19991214	18	Received-data bit synchronization circuit	375/371
126	US 6002709 A	19991214	37	Verification of PN synchronization in a direct-sequence spread-spectrum digital communications system	375/150

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110	Gatherer; Alan et al.
111	Hussein; Ershad et al.
112	de Lantremange; Maximilien d'Oreye
113	Yoneno; Kunio
114	Yonge, III; Lawrence W.
115	Nobusawa; Hideaki
116	Powell, II; Clinton C. et al.
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120	Oura; Hideto et al.
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127	US 5987064 A	19991116	18	Eye pattern display method, eye pattern display apparatus, and communications apparatus	375/228
128	US 5953367 A	19990914	25	Spread spectrum receiver using a pseudo-random noise code for ranging applications in a way that reduces errors when a multipath signal is present	375/147
129	US 5943379 A	19990824	26	Multi-phase trapezoidal wave synthesizer used in phase-to-frequency converter	375/374
130	US 5933454 A	19990803	17	Multi-carrier data transmissions system using an overhead bus for synchronizing multiple remote units	375/260
131	US 5930689 A	19990727	14	Apparatus and method for producing a plurality of output signals with fixed phase relationships therebetween	455/126
132	US 5905767 A	19990518	107	Timing recovery apparatus and a diversity communication apparatus using the same	375/355
133	US 5905764 A	19990518	14	Radio receiver	375/341
134	US 5898665 A	19990427	35	Coherent tracking apparatus and method for CDMA receiver	370/342
135	US 5850422 A	19981215	14	Apparatus and method for recovering a clock signal which is embedded in an incoming data stream	375/371
136	US 5832047 A	19981103	10	Self timed interface	375/356
137	US 5828676 A	19981027	62	Method and apparatus for robust communication based upon angular modulation	714/752
138	US 5815539 A	19980929	25	Signal timing synchronizer	375/371
139	US 5777998 A	19980707	15	Method and circuit arrangement for the realization of the higher path adaptation/mapping function in synchronous digital hierarchy/optical network equipment	370/509
140	US 5757857 A	19980526	22	High speed self-adjusting clock recovery circuit with frequency detection	375/271
141	US 5751775 A	19980512	16	Transmission circuit of a line encoded signal on a telephone line	375/371

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127	Kaku; Takashi et al.
128	Zhodzicshsky; Mark et al.
129	Wong; Hee et al.
130	Cioffi; John M.
131	Wilhite; Jeffrey B. et al.
132	Fujimura; Akinori
133	Watanabe; Hidekazu et al.
134	Sawahashi; Mamoru et al.
135	Chen; Dao-Long
136	Ferraiolo; Frank David et al.
137	Hurlbut; Amy O. et al.
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139	Traverso; Giovanni et al.
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142	US 5710649 A	19980120	22	Apparatus and methods for nulling non-random timing jitter in the transmission of digital optical signals	398/75
143	US 5699389 A	19971216	12	Oversampling correlator with virtual clock phase for a telecommunications device	375/371
144	US 5696800 A	19971209	29	Dual tracking differential manchester decoder and clock recovery circuit	375/361
145	US 5673295 A	19970930	10	Method and apparatus for generating and synchronizing a plurality of digital signals	375/356
146	US 5636249 A	19970603	8	Method of and apparatus for phase synchronization with an RDS signal	375/282
147	US 5610953 A	19970311	21	Asynchronous low latency data recovery apparatus and method	375/373
148	US 5587709 A	19961224	29	High speed serial link for fully duplexed data communication	341/100
149	US 5568526 A	19961022	10	Self timed interface	375/356
150	US 5557647 A	19960917	24	Baseband signal demodulator	375/371
151	US 5550876 A	19960827	9	Measuring device for a synchronous transmission system	375/371
152	US 5535252 A	19960709	20	Clock synchronization circuit and clock synchronizing method in baseband demodulator of digital modulation type	375/371
153	US 5533073 A	19960702	12	Method and an arrangement for minimizing a phase difference between two datastreams prior to changeover	375/371
154	US 5533072 A	19960702	22	Digital phase alignment and integrated multichannel transceiver employing same	375/371
155	US 5511091 A	19960423	13	Clock synchronization control check system	375/226
156	US 5491729 A	19960213	20	Digital phase-locked data recovery circuit	375/376
157	US 5485490 A	19960116	25	Method and circuitry for clock synchronization	375/371
158	US 5475715 A	19951212	18	Sync data introduction method and system	375/354
159	US 5459753 A	19951017	17	Method and apparatus for pattern independent phase detection and timing recovery	375/362

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143	Beladi; S. Hossein et al.
144	Berger; Lior
145	Read; Andrew J. et al.
146	Roither; Gerhard
147	Betts; Robert et al.
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149	Ferraiolo; Frank D. et al.
150	Kushige; Naohide et al.
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152	Kobayashi; Takahiro
153	Eriksson; Karl O.
154	Georgiou; Christos J. et al.
155	Saito; Naritoshi
156	Co; Ramon S. et al.
157	Leung; Wingyu et al.
158	Hase; Kenichi et al.
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160	US 5457719 A	19951010	12	All digital on-the-fly time delay calibrator	375/373
161	US 5452333 A	19950919	18	Digital jitter correction method and signal preconditioner	375/371
162	US 5452326 A	19950919	18	Digital PLL circuit with low power consumption	375/376
163	US 5414739 A	19950509	14	Transmission system constituted of multistage reproduction nodes	375/371
164	US 5400370 A	19950321	42	All digital high speed algorithmic data recovery method and apparatus using locally generated compensated broad band time rulers and data edge position averaging	375/371
165	US 5394443 A	19950228	22	Multiple interval single phase clock	375/371
166	US 5375147 A	19941220	22	Jitter compensating device	375/371
167	US 5359631 A	19941025	21	Timing recovery circuit for synchronous waveform sampling	375/376
168	US 5347548 A	19940913	11	Circuit for simultaneous recovery of bit clock and frame synchronization	375/371
169	US 5331667 A	19940719	23	Telephone exchange apparatus with communication line clocking	375/356
170	US 5331293 A	19940719	9	Compensated digital frequency synthesizer	331/1R
171	US 5327466 A	19940705	9	1X asynchronous data sampling clock	375/354
172	US 5321727 A	19940614	9	Signal phasing arrangement in a system for doubling the digital channel	375/347
173	US 5317602 A	19940531	15	Base-band delayed detector with synchronizing circuit	375/371
174	US 5291526 A	19940301	23	Digital signal reproducing apparatus for reducing influence by jitter	375/362
175	US 5278902 A	19940111	28	Method and apparatus for transition direction coding	380/42
176	US 5255292 A	19931019	13	Method and apparatus for modifying a decision-directed clock recovery system	375/368
177	US 5243630 A	19930907	10	Method of and arrangement for generating a clock signal from a biphase modulated digital signal	375/355

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160	Guo; Bin et al.
161	Guo; Bin et al.
162	Tanaka; Masato
163	Kobayashi; Naoya et al.
164	Guo; Bin
165	Byers; Larry L. et al.
166	Awata; Yutaka et al.
167	Behrens; Richard T. et al.
168	Messerges; Thomas S. et al.
169	Izumi; Michihiro
170	Shepherd; Wayne P. et al.
171	Marinaro; Frank
172	Bonnet; Jean-Marc et al.
173	Onoda; Masahiro et al.
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